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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,136	07/14/2003	David Mark	X-1269-1P US	6066

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
NGUYEN, JIMMY	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,136	MARK ET AL.	
	Examiner	Art Unit	
	Jimmy Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-18 and 20-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-18 and 20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Argument

The examiner acknowledges the terminal disclaimer filed 3/30/05, however upon further search the examiner found new ground of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3 – 11, 13 – 17, 23, 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Nicolai (US 5,198,707).

As to claim 1, Nicolai discloses (fig 1) a test configuration comprising:

an integrated circuit to be tested (the structure of figure 1);

an I/0 pad (10) of the integrated circuit;

an output buffer (14), wherein an output terminal of the output buffer (14) is coupled to the I/0 pad (10);

a current injector (S1) on the integrated circuit coupled to the 1/0 pad (10) for injecting a current at the I/0 pad (10); and

a detector (column 3 lines 1 – 38) on the integrated circuit coupled to the I/0 pad (10) for detecting a logic level (see the abstract) of the 1/0 pad.

As to claims 3, 16, Nicolai discloses (fig 1) the test configuration of claim 1 wherein the output buffer is a tristate buffer (14).

As to claims 4, 23, Nicolai discloses (fig 1) the test configuration of claim 1 further comprising an input buffer (S1), wherein an input terminal (A) of the input buffer is coupled to the 1/0 pad (10).

As to claim 5, Nicolai discloses (fig 1) the test configuration of claim 1 wherein the current injector (S1) selectively enabled by a memory bit (sequencer).

As to claim 6, Nicolai discloses (fig 1) the test configuration of claim 1 wherein the current injector (S1) is a resistive element on the IC coupled between the I/O pad (10) and a voltage reference node (Vcc).

As to claim 7, Nicolai discloses (fig 1) the test configuration of claim 1 wherein the resistive element is a transistor (S1).

As to claim 8, Nicolai discloses (fig 1) the test configuration of claim 1 wherein a gate of the transistor (S1) is coupled to a memory bit (the sequencer is control the enabling of the all the switches or transistors).

As to claims 9, 10, Nicolai discloses (fig 1) the test configuration of claim 1 wherein the voltage reference node is a power node (Vcc) and ground node (B node).

As to claim 11, Nicolai discloses (fig 1) the test configuration of claim 1 wherein the IC is one of a plurality of IC on wafer.

As to claim 13, Nicolai discloses (fig 1) the test configuration of claim 1 wherein the IC is a programmable logic device.

As to claims 14, 24, Nicolai discloses (fig 1) the test configuration of claim 1 wherein the detector is a boundary scan cell.

As to claim 15, Nicolai discloses (fig 1) a test configuration comprising:

an integrated circuit to be tested (the structure of figure 1);

an I/0 pad (10) of the integrated circuit;

an output buffer (14), wherein an output terminal of the output buffer (14) is coupled to the I/0 pad (10);

a current injector (S1) on the integrated circuit coupled to the 1/0 pad (10) for injecting a current at the I/0 pad (10);

wherein the current injector is a first transistor (S1) coupled between the I/O pad (10) and a power node (Vcc);

a detector (column 3 lines 1 – 38) on the integrated circuit coupled to the I/0 pad (10) for detecting a logic level (see the abstract) of the 1/0 pad.

a second transistor (S2) coupled between the I/O pad (10) and a ground node (B);

a first memory bit (6)coupled to a gate of the first transistor (S1); and

a second memory bit (7) coupled to a gate of the second transistor (S2).

As to claim 17, Nicolai discloses (fig 1) a method for testing an I/0 pad of an integrated circuit, the method comprising:

enabling a current injector (S1, by sequencer) on the integrated circuit coupled to the I/0 pad;

driving an output value at the I/0 pad through an output buffer (14) coupled to the I/0 pad (10)

enabling a detector (column 3 lines 1 – 38) on the integrated circuit coupled to the 1/0 pad (10) ; and

after enabling the detector, detecting a logic value (18) of the 1/0 pad (10).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12, 25, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicolai (US 5,198,707) in view of Rutten (US 6,747,469).

As to claim 12, 25, 26, Nicolai discloses everything except for a probe card coupled to a subset of the plurality of I/O pads; and ate coupled to the probe card.

On the other hand, Rutten teaches (fig 1) a probe card (140) coupled to a subset (150) of the plurality of I/O pads ; and ate (110) coupled to the probe card (140).

It would have been obvious to one having an ordinary skill in art at the time of the invention was made to modify the test configuration structure with the probe card and ate for the purpose of the transmitting the signal and testing the dut.

5. Claims 18, 20 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicolai (US 5,198,707) in view of Fister (US 6,285,609).

As to claims 18, 20 - 22, Nicolai discloses everything except for comparing the detected logic value with an expected value; and

If the detected logic value and the expected value do not match, rejecting the IC.

On the other hand, Fister teaches comparing (column 5 lines 40 – 48) the detected logic value with an expected value; and

If the detected logic value and the expected value do not match (column 5 lines 40 – 48), rejecting the IC.

It would have been obvious to one having an ordinary skill in art at the time of the invention was made to compare the logic value for the purpose of recognizing the testing result.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen whose telephone number is 571-272-1965. The examiner can normally be reached on M-F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ramtez Nestor can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jimmy Nguyen

6/6/05

VINH NGUYEN
PRIMARY EXAMINER
A.U. 2829
06/09/05